UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,373	01/09/2001	Cary Ussery	IMP-002 (8326/5))	6632

21323 7590 06/28/2004

TESTA, HURWITZ & THIBEAULT, LLP
HIGH STREET TOWER
125 HIGH STREET
BOSTON, MA 02110

EXAMINER	
KIK, PHALLAKA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/757,373	USSERY ET AL.	
	Examin r	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on th cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action responds to Applicant's amendment filed on 10/3/2003.

Claims 1-35 are pending, wherein claims 1,8,10,17-19,22,27,28 have been amended.

Claims 1-35 have been examined; however, Applicant's arguments are not persuasive. Therefore, the previous Office Action is incorporated herein. The claims are also newly rejected to as being necessitated by Applicant's amendment.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1- 9, 11, 13, 16 - 20, 22, 24, 27, 28, 30, 33 and 35** are rejected under 35 U.S.C. 102(e) as being anticipated by **Ussery et al.** (US Patent No. 6,075,935).

The applied reference has common inventors and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e)

might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per **claim 1**, **Ussery et al.** discloses in Fig. 2, Fig. 5 and column 8, lines 43 - 49, a designer configurable processor (200) comprising:

a. a plurality of desirer configurable computational units (218, 220 and 222) operating in parallel;

b. a memory device (202, 203 and 214) that communicates with the plurality of computational units through a data communication module (206); and

c. a software development tool (50) that configures the plurality of computational units and a data path though the data communication module.

As per **claim 2**, **Ussery et al.** discloses in Fig. 5 and column 3, lines 4 - 5 the designer configurable processor comprising a Very Long Instruction Word (VLIWI processor task engine.

As per **claim 3**, **Ussery et al.** discloses in Fig. 5 the data communication module comprising a register routed data communication module.

As per **claim 4**, **Ussery et al.** discloses in Fig. 5 and column 8, lines 50 - 55 the memory device (214) storing at least one of data and instruction code.

As per **claim 5**, **Ussery et al.** discloses in Fig. 5 and column 8, lines 36 - 43 a task queue (208) that communicates with the data communication module, the task queue scheduling tasks for the processor.

As per **claim 6**, **Ussery et al.** discloses in Fig. 5 the task queue comprising a task queue controller module (212) that communicates with the data communication module and a task queue module that communicates with task queue bus (210).

As per **claim 7**, **Ussery et al.** discloses in Fig. 5 an instruction memory (214) that communicates with the task queue controller module, the instruction memory storing tasks for the processor.

As per **claim 8**, **Ussery et al.** discloses in Fig. 2 the software development tool comprising at least one of a compiler (52), an assembler, an instruction set simulator, or a debugging environment.

As per **claim 9**, **Ussery et al.** discloses in Fig. 2 and column 5, lines 3 - 17 the software development tool comprising a graphical interface (62) that visually illustrates the configuration of the processor.

As per **claim 11**, **Ussery et al.** discloses in Fig. 2 and Fig. 4 the software development tool configuring a data path from the processor to an input/output module.

As per **claim 13**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 the software development tool configuring a data routing path of at least one of the plurality of computational units.

As per **claim 16**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 the software development tool configuring an instruction set of at least one of the plurality of computational units.

As per **claim 17**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 at least one of the

plurality of desirer configurable computational units (222) comprising a set of input registers and a set of result registers.

As per **claim 18**, **Ussery et al.** discloses in Fig. 2, Fig. 4 and Fig. 5 a designer configurable multi-processor system comprising:

a. a plurality of designer configurable processors (152 and 154), each of the plurality of processors comprising a plurality of desirer configurable computational units (218, 220 and 222) operating in parallel;

b. a memory device (202, 203 and 214) that communicates with the plurality of computational units through a data communication module;

c. an input/output (I/O) module (160) that communicates with at least one of the plurality of processors through an I/O bus; and

d. a software development tool (50) that configures the multi-processor system.

As per **claim 19**, **Ussery et al.** discloses in Fig. 5 and column 3, lines 4 - 5 at least one of the plurality of processors comprising a Very Long Instruction Word (VLIW) processor.

As per **claim 20**, **Ussery et al.** discloses in Fig. 4 an instruction memory device (156) that communicates with at least one of the plurality of processors.

As per **claim 22**, **Ussery et al.** discloses in Fig. 4 the software development tool configuring a data path to the I/O module (160).

As per **claim 24**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 the software development tool configuring a data routing path of at least one of the plurality of computational units.

As per **claim 27**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 the software development tool configuring an instruction set of at least one of the plurality of computational units.

As per **claim 28, Ussery et al.** discloses in Fig. 2, Fig. 5 and column 3, lines 4 - 5 a method of defining a computational unit for a multi-processor hardware system, the method comprising:

a. defining an architecture (200) of at least computation unit (218) in a Very Long Instruction Word IVLIWI processor with a software development tool (50); and

b. generating data from the software development tool that integrates the at least one computation unit into the VLIW processor task engine.

As per **claim 30**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 defining an internal data routing path of the at least one computation unit with the software development tool.

As per **claim 33**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 defining an instruction set of the at least one computation unit with the software development tool.

As per **claim 35**, **Ussery et al.** discloses in Fig. 2 and Fig. 5 the generating data from the software development tool comprising generating scripts for an electronic design automation tool.

4. **Claims 1-8,11-13,16-20,22-24,27-30,33,35** are rejected under 35 U.S.C. 102(b) as being anticipated by **Iseli et al.** ("Spyder: a reconfigurable VLIW processor using FGPAs", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 17-24).

As per **claim 1,3,18**, the elements of the claims are illustrated in Fig. 2 (page 19), wherein the designer configurable computational units operating in parallel correspond to EU1, EU2, and EU3 (see page 18, section 2), the memory device corresponds to "Memory Data" unit and/or "Microcode Memory" unit which communicate with the computation units through data communication module (e.g., at least Transfer and Register bank A, B units (register routed), and/or host computer--see page 20, including datapath configuration is also described as part of the execution units and the memory-registers transfer interface), wherein the software development tool includes the compiler and other software that allows the user to custom configure the computational units and data paths (i.e., interconnection network--see Fig. 1, page 18) as further described on page 18, section 2 as part of the user designing and implementing the new operator, add it to the library so that the compiler can generate the proper instruction to make use of it for designer customization of the computational units.

As per **claims 2,19**, the VLIW process task engine being part of the configurable processor is also discussed on page 19 (column 1, 4th paragraph).

As per **claims 4,20**, the memory storing data and instruction code (instruction memory) is described on pages 20 and 22 (section 3, phases 3 and 4) wherein the interactions of the register, memory and execution units show that both instruction codes for the execution units and data for and resulting from the execution units are stored in the memory as well.

As per **claims 5-7,22-24**, the task queue for scheduling tasks for the processor is part of the instruction execution described in section 3 (pages 20-22).

As per **claim 8**, at least the assembler (micro-assembler--page 18, first column, 3rd paragraph), compiler (page 18, 2nd column), and instruction set simulator (e.g., instruction execution, section 3) are described as part of the software development tool.

As per **claims 11-13**, the configuration of the data path from the processor to an input/output module, including the width (e.g., controls by the configurable register) and routing of the computational unit, is also described as part of the execution units and the memory-registers transfer interface (page 20).

As per **claims 16,27,33**, the software development tool which configures an instruction set of at least one of the plurality of computational units is part of the compiling and assembling process which necessarily configures the particular instructions for the configurable or computational units in order to execute the computational units (see page 18).

As per **claim 17**, the input registers and results registers being part of the configurable computing units are also described in illustrated in Fig. 3 (page 21).

As per **claim 28**, all of the elements of the claims are discussed in the rejection of claims 1 and 2 above.

As per **claims 29-30**, all of the elements of the claims are discussed in the rejection of claims 11-13 above.

As per **claim 35**, the scripts for the electronic design tool generated is also inherently part of the output of the compiler, as is well known in the art (see page 18).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 10,21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ussery et al.** (US Patent No. 6,075,935) in view of **Killian et al.** (US Patent No. 6,477,683).

The applied reference has a common inventor/assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the

reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claims 10,21**, **Ussery et al.** discloses all of the elements of the claims as discussed in the rejections of claims 1 and 18 above, but failed to teach the software development tool generating a synthesizable RTL description of the processor. Such software development tool is taught by **Killian et al.** (see column 32, lines 49 - 60). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify **Ussery et al.** to use the synthesizable RTL description as taught by **Killian et al.** because such modification would at least provide for the purpose of obtaining a FPGA implementation from high level language descriptions (**Killian et al.**, column 32, lines 55-56).

7. **Claims 9,10,21** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Iseli et al.** ("Spyder: a reconfigurable VLIW processor using FGPAs", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 17-24) in view of **Killian et al.** (US Patent No. 6,477,683).

As per **claim 9**, **Iseli et al.** discloses all of the elements of the claims as discussed in the rejections of claim 1 above, but failed to teach the graphical interface (GUI) that visually illustrates the configuration of the processor. Such GUI for visually illustrating the configuration of the processor is taught by **Killian et al.** (see). It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the GUI as taught by **Killian et al.** into the system of **Iseli et al.**

because incorporation would allow the user to interactively configures the processor as intended by the **Iseli et al.**.

As per **claims 10,21**, **Iseli et al.** discloses all of the elements of the claims as discussed in the rejections of claims 1 and 18 above, but failed to teach the software development tool generating a synthesizable RTL description of the processor. Such software development tool is taught by **Killian et al.** (see column 32, lines 49 - 60). It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify **Iseli et al.** to use the synthesizable RTL description as taught by **Killian et al.** because such modification would at least provide for the purpose of obtaining a FPGA implementation from high level language descriptions (**Killian et al.**, column 32, lines 55-56).

8. **Claims 12,13,29** are rejected under 35 U.S.C. 103(a) as being obvious over **Ussery et al.** (US Patent No. 6,075,935) in view of **Rupp** (US Patent No. 5,784,636).

The applied reference has a common inventor/assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application

and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claims 12,23,29**, **Ussery et al.** discloses the claimed as discussed in the rejection of claims 11,22 above, but failed to teach that the software development tool configures a width of the data path from the processor to the input/output module. However, **Rupp** teaches in column 37, lines 42 - 52 a software development tool configuring a width of a data path from a processor to an input/output module. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Ussery et al.** by using the width of a data path as taught by **Rupp** because modification would at least allow the defining of the memory speed.

9. **Claims 14,25,32** are rejected under 35 U.S.C. 103(a) as being obvious over **Ussery et al.** (US Patent No. 6,075,935) in view of **Greenbaum et al.** (US Patent No. 5,933,642).

The applied reference has a common inventor/assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed

but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claims 14,25,32**, **Ussery et al.** discloses the claimed invention as discussed in the rejections of claims 1, 18 and 28 above; but failed to disclose the software development tool that configures an instruction execution speed of at least one of the plurality of computational units. However, **Greenbaum et al.** teaches in column 3, lines 25 - 45 a software development tool configuring an instruction execution speed of at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Ussery et al.** using the execution speed as taught by **Greenbaum et al.** because such modification would properly coordinates the particular computational units in the

configurable logic resources into the system (**Greenbaum et al.**, column 3, lines 25 - 26).

10. **Claims 14,25,32** are rejected under 35 U.S.C. 103(a) as being obvious over **Iseli et al.** ("Spyder: a reconfigurable VLIW processor using FGPAs", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 17-24) in view of **Greenbaum et al.** (US Patent No. 5,933,642).

As per **claims 14,25,32**, **Iseli et al.** discloses the claimed invention as discussed in the rejections of claims 1, 18 and 28 above; but failed to disclose the software development tool that configures an instruction execution speed of at least one of the plurality of computational units. However, **Greenbaum et al.** teaches in column 3, lines 25 - 45 a software development tool configuring an instruction execution speed of at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Iseli et al.** by using the execution speed as taught by **Greenbaum et al.** because such modification would properly coordinates the particular computational units in the configurable logic resources into the system (**Greenbaum et al.**, column 3, lines 25 - 26).

11. **Claims 15,26,31** are rejected under 35 U.S.C. 103(a) as being obvious over **Ussery et al.** (US Patent No. 6,075,935) in view of **Suzuki** (US Patent No. 5,764,857).

The applied reference has a common inventor/assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed

but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claims 15,26,31**, **Ussery et al.** discloses the claimed invention as discussed in the rejection of claims 1, 18 and 28 above, but failed to teach the software development tool that configures an energy required to operate at least one of the plurality of computational units. However, **Suzuki** teaches in column 4, lines 25 - 39 a software development tool configuring an energy required to operate at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Ussery et al.** by using the energy required as taught by **Suzuki** because such modification would make efficient use of power in executing each of the programs with the computer.

12. **Claims 15,26,31** are rejected under 35 U.S.C. 103(a) as being obvious over **Iseli et al.** ("Spyder: a reconfigurable VLIW processor using FGPAs", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 17-24) in view of **Suzuki** (US Patent No. 5,764,857).

As per **claims 15,26,31**, **Iseli et al.** discloses the claimed invention as discussed in the rejection of claims 1, 18 and 28 above, but failed to teach the software development tool that configures an energy required to operate at least one of the plurality of computational units. However, **Suzuki** teaches in column 4, lines 25 - 39 a software development tool configuring an energy required to operate at least one of plurality of computational units. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Iseli et al.** by using the energy required as taught by **Suzuki** because such modification would make efficient use of power in executing each of the programs with the computer.

13. **Claim 34** is rejected under 35 U.S.C. 103(a) as being obvious over **Ussery et al.** (US Patent No. 6,075,935) in view of **Enokido et al.** (US Patent No. 5,933,634).

The applied reference has a common inventor/assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not

claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

As per **claim 34**, **Ussery et al.** discloses the claimed invention except for performing a consistency check to validate the multi-processor hardware system. However, **Enokido et al.** teaches in column 2, lines 27 - 43 performing a consistency check to validate a multi-processor hardware system. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Ussery et al.** by using the consistency check as taught by **Enokido et al.**. because such modification would insures that the system of **Ussery et al.** functions as desired.

14. **Claim 34** is rejected under 35 U.S.C. 103(a) as being obvious over **Iseli et al.** ("Spyder: a reconfigurable VLIW processor using FGPAs", 1993 Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines, 5 April 1993, pp. 17-24) in view of **Enokido et al.** (US Patent No. 5,933,634).

As per **claim 34**, **Iseli et al.** discloses the claimed invention as discussed in the rejection of claim 28 above, but failed to teach performing a consistency check to

validate the multi-processor hardware system. However, **Enokido et al.** teaches in column 2, lines 27 - 43, teaches performing a consistency check to validate a multi-processor hardware system. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify **Iseli et al.** by using the consistency check as taught by **Enokido et al.** because such modification would insures that the system of **Iseli et al.** functions as desired.

Remarks

15. The objections to the drawings due to the noted minor informalities are withdrawn as being corrected by Applicant's amendment to the specification, filed on 10/3/2003.

16. The objections to the disclosure due to the noted informalities are withdrawn as being corrected by Applicant's amendment filed on 10/3/2003.

17. As per **claims 1- 9, 11, 13, 16 - 20, 22, 24, 27, 28, 30, 33 and 35**, Applicant argued that the claims as newly amended are patentable over **Ussery et al.**, alone or in view of **Killian et al.**, **Rupp**, **Greenbaum et al.**, **Suzuki**, and/or **Enokido et al.**, wherein the prior arts made of record failed to teach or suggest the software development tool which allows the designer to custom configure the plurality of computational units and a data path through the data communication module, wherein **Ussery et al.** teaches selecting from a set data paths to eliminate time intensive analysis of possible paths; **Killian** itself creates its version of optimal datapaths, not the designer; **Rupp** teaches using a preset number of data paths instead of the recited custom configurable data paths; **Greenbaum**'s selectable hardware organization between a plurality of hardware architectures in which the selection between predefined hardware choices does not

equal the recited customizable data paths; **Suzuki** and **Enokido** further fails to teach or suggest the custom configurable data paths. The Examiner is not persuaded. Applicant's claims only calls for a software development tool for enabling a designer to custom configure the plurality of computational units and a data path through the data communication module, which Applicant's arguments seem to interpret the development tool in which the designer is able to directly and manually configure the particular computational units and data path. This interpretation is not considered the broadest interpretation of the claims for one of ordinary skilled in the art since the configuration technology would necessarily customizes computational units (e.g., FPGA or programmable logic devices) to implement the user's or designer's circuit design, wherein as long as the designer or user is involve in the design process, the designer or user directly or indirectly affects or enables the customization of the computational units (and their data paths) (see **Agrawal, Om P. et al.**, US Patent No. 6,216,257, especially col. 3, lines 9-61; **Killian, Earl A. et al.**, US Patent No. 6,477,683, especially col. 9, line 56 to col. 10, line 5). In **Ussery et al.**, the computational units and data path(s) are configured to implement the particular user's/designer's circuit design which was inputted by the user at the higher level description which is then automatically generated into the particular custom configuration implementation; thus indirectly enabling user/designer to custom configure the computational units and data path(s) from the higher description level. This software development tool is further defined in applicant's claimed invention as at least one of a compiler, an assembler, an instruction set simulator, or a debugging environment (see claim 8). Furthermore, as given in the

new rejections above, **Iseli et al.** anticipate the claims wherein the designer (user) is allowed to design and implement a new operator (i.e., custom configure the computational units and/or datapaths) using some sort of software tool since the method/system is a computer-implemented method/system, and then added to the library and have the compiler make use of it (see page 18, column 2); thus enabling the user to custom configure the computational units and data path(s).

18. As per **claims 10,12,14-15,21,23,25-26,29,31-32,34**, Applicant argued that **Killian et al.**, **Rupp, Greenbaum**, and **Suzuki** failed to remedy the deficiencies of **Ussery** in enabling custom configuring of the computational units and datapath as claimed. Since **Ussery** does allow enabling custom configuring of the computational units and datapath as claimed, as discussed above, the rejections in view of teachings of **Killian et al.**, **Rupp, Greenbaum**, or **Suzuki** are proper. Furthermore, the new rejections based on **Iseli et al.** in view of these prior arts are similarly applicable since **Iseli et al.** also provides for all of the elements of the claims from the rejected claims based on these prior arts depend, including the enabling custom configuring of the computational units and datapath.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Therefore, Applicant is herein requested to consider them carefully in response to this Office Action.

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 7:30AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-1450

or faxed to:

703-872-9318 (for Before-Final) and 703-872-9319 (for After-Final) for formal communications intended for entry,

Or:

(571) 273-1895 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing).

22. **Applicant should note that effective May 1, 2003, the United States Patent and Trademark Office has a new Commissioner for Patents address for transitioning to the new Office location in Alexandria, VA, wherein**

correspondence in patent-related matters to organizations reporting to the Commissioner for Patents must now be addressed to:

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PK
June 23, 2004

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800